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EXAMINER

TRAN, THUY V

ART UNIT

PAPER NUMBER

2821

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/023,213	STACK, TOM
	Examiner THUY V. TRAN	Art Unit 2821

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 17 December 2001.

2a) This action is **FINAL**.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 25-28 and 30-38 is/are allowed.

6) Claim(s) 1-4,9-11,16,17,23,29 and 39 is/are rejected.

7) Claim(s) 5-8,12-15,18-22 and 24 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 17 December 2001 is/are: a) accepted or b) objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) All b) Some \* c) None of:

        1. Certified copies of the priority documents have been received.

        2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

        3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    \* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## **DETAILED ACTION**

Claims 1-39 are currently presented in the instant application according to the Applicant's filing on December 17<sup>th</sup>, 2001.

The Applicant is noted that the numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims A15 and 23 have been renumbered 23 and 24, respectively.

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on July 30<sup>th</sup>, 2002 is in compliance with the provisions of 37 CFR 1.97 and 1.98. Therefore, this information disclosure statement has been considered.

### ***Drawings Objections***

2. The drawings are objected to because the drawing lines and reference numerals in Fig. 7 are not uniform and legible. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Objections/ Minor Informalities***

3. Claims 1-2, 6-7, 23, 25-27, 29-32, 34, and 39 are objected to because of the following informalities:

Claim 1, line 13, change "a" to --the--;

Claim 1, line 14, insert --detected-- between "the" (first occurrence) and "voltage" (first occurrence);

Claim 2, line 1, change "voltage-responsive" to --shut-off--;

Claim 6, line 3, insert --field-- between "first" and "effect";

Claim 7, line 1, change "voltage-responsive" to --shutoff--;

Claim 23, line 2, change "the" to --a--;

Claim 25, line 5, insert --sensed-- after "the" (third occurrence);

Claim 26, line 1, change "the" to --a--;

Claim 27, line 2, change "ballast circuit" to --inverter--; and change "the" (second occurrence) to --a--;

Claim 27, line 3, change "the" (first occurrence) to --a--; and change "a" to --the--;

Claim 29, line 5, insert --configured-- between "circuit" and "between";

Claim 29, line 10, insert --sensed-- between "the" and "voltage";

Claim 30, line 5, insert --circuit-- between "input" and "and"; and insert --circuit-- between "output" and "for";

Claim 31, line 3, insert --at least one-- between "the" and "transistor";

Claim 32, line 2, insert --at least one-- between "the" (second occurrence) and "transistor";

Claim 34, line 3, insert --at least one-- between "the" and "transistor";

Claim 39, line 3, insert --to-- between "coupled" and "the";

Claim 39, line 4, replace "from" with --coupled to--; and

Claim 39, line 10, change "a" to --the--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 9, 16-17, 23, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Ribarich (U.S. Patent No. 5,451,845).

With respect to claim 1, Ribarich discloses, in Figs. 1 and 4, a ballast circuit comprising (1) a DC input circuit (*which comprises an output of the full wave rectifier and a filter; see Fig. 1 and col. 3, lines 14-15*) having a high voltage line (*which is the upper line of the Fig. 1 circuit*) and a base line (*which is the lower line of the Fig. 1 circuit*), (2) a lamp drive circuit (*included in load circuit [12] with an electric discharge lamp; see col. 3, lines 9-10 and 55-58*) coupled between the high voltage line and the base line, (3) an output circuit [D1, L, 13, R, D2, C] coupled to the lamp drive circuit (*see Fig. 1*) for producing a lamp drive current used for driving an electric discharge lamp (*regarding the electric discharge lamp, which is included in the load circuit [12] with its driving circuit, see col. 3, line 10*), and (4) a ballast protection circuit [10] (*see Fig. 1*) for protecting the lamp drive circuit comprising (i) a detection circuit [ZD1] (*see Figs. 1 and 4; called detection circuit since the Zener diode [ZD1] determines or senses a maximum value of the input voltage from the power source [U1]; see col. 4, lines 59-61*) coupled between the high voltage line and the base line (*see Figs. 1 and 4; wherein the terminal [1] is connected to the high voltage line, and the terminals [3, 4] are connected to the base line*) and

configured to detect when a voltage on the high voltage line exceeds a threshold (*see col. 4, lines 59-63*), and (ii) a shutoff device [S1] coupled to the detection circuit [ZD1] (*via R5, C5, R1; see Fig. 4*) and to the lamp drive circuit (*see Figs. 1 and 4*) for preventing the lamp drive circuit from producing the lamp drive current when the detected voltage on the high voltage line exceeds the threshold (*see Figs. 1 and 4; col. 3, lines 44-48*).

With respect to claim 2, Ribarich discloses that the shutoff device [S1] is a bipolar transistor (*which is one of a silicon control rectifier, a MOSFET, a bipolar transistor, and an opto-isolator, as claimed; see col. 4, lines 8-10*).

With respect to claim 3, Ribarich discloses that the ballast protection circuit (of Fig. 4) includes a delay circuit [C5, R5] (*or wherein at least one of the ballast protection circuit and the shutoff device includes a delay circuit [C5, R5] as claimed; see Fig. 4; col. 4, lines 52-53*).

With respect to claim 4, Ribarich discloses that the delay circuit includes a capacitor [C5] coupled to a resistor [R5] (*see Fig. 4*).

With respect to claim 9, Ribarich discloses that the ballast circuit further includes a full wave rectifier (*which is part of power source [U1]; see col. 3, lines 14-15*) coupled to the DC input circuit at the high voltage line and the base line (*which comprises an output of the full wave rectifier and a filter; see Fig. 1 and col. 3, lines 14-15*).

With respect to claim 16, Ribarich discloses that the detection circuit [ZD1] is configured to detect an inherent voltage having a value of 400 Volts, or greater than 200 Volts as claimed (*since the open/close activation of the shutoff device or switch [S1] relates to the voltage detection of [ZD1]; see col. 3, lines 65-67*).

With respect to claim 17, Ribarich discloses that the detection circuit [ZD1] is configured to detect an inherent voltage having a value of 400 Volts, or greater than 212 Volts as claimed (*since the open/close activation of the shutoff device or switch [S1] relates to the voltage detection of [ZD1]; see col. 3, lines 65-67*).

With respect to claim 23, Ribarich discloses that the shutoff device [S1] includes a bipolar transistor, *which is a component selected from a group of a silicon control rectifier, a MOSFET, a bipolar transistor, and an opto-isolator, as claimed (see col. 4, lines 8-10)*.

With respect to claim 39, Ribarich discloses, in Figs. 1 and 4, a ballast circuit comprising (1) a DC input circuit (*which comprises an output of the full wave rectifier and a filter; see Fig. 1 and col. 3, lines 14-15*), (2) a lamp drive circuit (*included in load circuit [12] with an electric discharge lamp; see col. 3, lines 9-10 and 55-58*) coupled to the DC input circuit (*see Fig. 1*), (3) an output circuit [D1, L, 13, R, D2, C] coupled to the lamp drive circuit (*see Fig. 1*) for producing a lamp drive current used for driving an electric discharge lamp (*regarding the electric discharge lamp, which is included in the load circuit [12] with its driving circuit, see col. 3, line 10*), and (4) a ballast protection circuit [10] (*see Fig. 1*) for protecting the lamp drive circuit including (i) a detection circuit [ZD1] (*see Figs. 1 and 4; called detection circuit since the Zener diode [ZD1] determines or senses a maximum value of the input voltage from the power source [U1]; see col. 4, lines 59-61*) coupled to the DC input circuit (*see Figs. 1 and 4; wherein the terminal [1] is connected to the high voltage line, and the terminals [3, 4] are connected to the base line*) and configured to detect when a voltage from the DC input circuit exceeds a threshold (*see col. 4, lines 59-63*), and (ii) a shutoff device [S1] coupled to the detection circuit [ZD1] (*via R5, C5, R1; see Fig. 4*) and to the lamp drive circuit (*see Figs. 1 and 4*) for preventing

the lamp drive circuit from producing the lamp drive current (*see Figs. 1 and 4; col. 3, lines 44-48*).

6. Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Yagi et al. (U.S. Patent No. 5,140,229).

With respect to claim 29, Yagi et al. discloses, in Figs. 1-2, a ballast circuit comprising (1) an input circuit [9] for receiving current from a current source (*provided by power source [2] through supply lines [4, 4']*; *see Figs. 1 and 2*), (2) an output circuit [10] for supplying power to an electric discharge lamp [16] (*see Figs. 1 and 2*), and (3) a ballast protection circuit [19, 19', 20, 22, 34, 23, 29, 54, 21] configured between the input and output circuits [9 and 10, respectively] for protecting the ballast circuit from providing excessive power at the output circuit (*see col. 1, lines 55-58*); the ballast protection circuit includes (i) a voltage sensing circuit [29] (*see Fig. 2; col. 4, lines 20-22*) for sensing a voltage in the input circuit [9], and (ii) a response circuit [54] coupled to the voltage sensing circuit [29] (*see Fig. 2*) for reducing the power (*via results provided by the current detecting circuit [34] and voltage detecting circuit [29]*; *see Fig. 2*) provided by the output circuit when the sensed voltage reaches a given level (*by feeding the pulses through the gate drives [21] to the gate of the FET [26] of the input circuit [9] for controlling the output voltage thereby resulting in lowering/reducing the power provided by the output circuit and to the lamp*; *see Fig. 2; col. 1, lines 55-58; col. 4, lines 20-44; col. 5, lines 39-45*).

#### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ribarich (U.S. Patent No. 5,451,845) in view of Coaton et al. (Lamps and lighting, Fourth Edition, Published in Great Britain in 1997; pages 322-323).

With respect to claim 10, Ribarich discloses all of the claimed limitations, as expressly recited in claim 1, except for specifying that an inverter circuit be included in the lamp drive circuit.

Coaton et al. discloses, in Fig. 17.19(b), a lamp drive circuit, which comprises an inverter circuit [T1, T2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the lamp drive circuit of Ribarich with an inverter circuit to perform a DC-AC conversion in order to properly operate the lamp since such a configuration of the inverter circuit in the lamp drive circuit for the stated purpose has been a well-known practice in the art as evidenced by the teachings of Coaton et al. (*see Coaton et al.; page 322, lines 8-13*).

With respect to claim 11, the combined teachings of Ribarich and Coaton et al. disclose that the inverter circuit [T1, T2] includes transistors [T1, T2] in a push-pull configuration (*see Coaton et al.; page 322, Fig. 17.19(b)*).

#### ***Allowable Subject Matter***

9. Claims 25-28 and 30-38 would be allowed. However, the Applicant is noted that claims 25-27, 30-32, and 34 should be corrected to overcome the objections set forth in this Office Action and thus to make clear the claimed invention.

10. Claims 5-8, 12-15, 18-22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant is noted that claims 6-7 should be corrected to overcome the objections set forth in this Office Action and thus to make clear the claimed invention.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to disclose or suggest (1) the output circuit includes an inverter comprising first and second field effect transistors in a push-pull configuration including a feedback device for causing the inverter to generate an oscillating lamp drive current, as called for in claim 5, (2) the arrangement of a pair of MOSFETs in the inverter circuit, as called for in claim 12, (3) the shutoff device includes an SCR, as called for in claim 13, (4) the detection circuit is configured to detect when a voltage on the high voltage line exceeds a value equal to approximately twice the voltage on the high voltage line under normal operating conditions, as called for in claim 15, (5) the detection circuit includes a series of diodes, as called for in claim 18, (6) the lamp drive circuit includes a MOSFET and the shutoff device is coupled to a gate of the MOSFET, as called for in claim 24, (7) a method of protecting a ballast circuit having an inverter from generating an excessive lamp drive current comprising a step of sensing an input voltage that varies as a function of an input to the ballast, as called for in independent claim 25, and (8) an arrangement including (i) an oscillation circuit between the input circuit and output circuit for creating an oscillating current for the output circuit to drive the electric discharge lamp, and (ii) a protection circuit including at least one diode and a trigger circuit coupled to

each other for reducing the drive current in the output circuit when a voltage in the input circuit reaches a given level, as called for in independent claim 30.

*Citation of relevant prior art*

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Ito et al. (U.S. Patent No. 6,534,930) discloses a discharge lamp lighting circuit with a protection circuit.

Prior art Lau (U.S. Patent No. 6,181,084) discloses a ballast circuit for high intensity discharge lamps.

Prior art Yamashita et al. (U.S. Patent No. 6,087,776) discloses a discharge lamp lighting circuit with a protection circuit.

Prior art Kern (U.S. Patent No. 6,081,104) discloses a discharge lamp lighting circuit system.

Prior art Konopka et al. (U.S. Patent No. 5,770,925) discloses an electronic ballast with inverter protection and re-lamping circuits.

Prior art Kling et al. (U.S. Patent No. 5,150,09) discloses an electric circuit for discharge lamp in which a Zener diode is used for sensing when the voltage exceeds a desired predetermined value.

*Inquiry*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THUY V. TRAN whose telephone number is (703) 305-0012. The examiner can normally be reached on M-F (8:30-6:00) First Friday Off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DON K. WONG can be reached on (703) 308-4856. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

THUY V. TRAN  
Examiner  
Art Unit 2821

T.T.  
June 30, 2003

A handwritten signature in black ink, appearing to read "Thuy Tran".